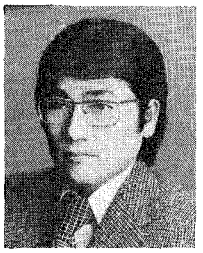

worked on research and development of silicon and gallium arsenide microwave devices, including planar analog transistors. In 1975 he transferred to the Fujitsu Laboratories, Ltd., Kawasaki, Japan, where he has been engaged in the research and development of compound semiconductor high-speed devices, including high electron mobility transistors (HEMT's). In 1981 he received the prize of the Minister of Science and Techniques in Japan for the invention of a HEMT.

Mr. Mimura is a member of the Physical Society of Japan.

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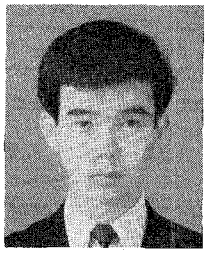

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Mr. Yokoyama is a member of the Physical Society of Japan, the Japan Society of Applied Physics, and the Institute of Electronics and Communication Engineers of Japan.

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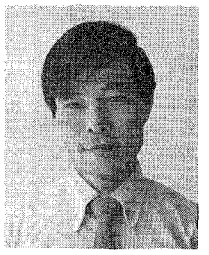

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Mr. Ishikawa is a member of the Institute of Electronics and Communication Engineers of Japan and the Electrochemical Society.

A GaAs MSI Word Generator Operating at 5 Gbits/s Data Rate

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Abstract—**This paper describes a monolithic MSI GaAs word generator that operates at data rates from a few bits/s up to 5 Gbits/s. This circuit, with 600 active devices, consists of an 8:1 parallel-to-serial converter, a timing generator, control logic, and ECL-interface networks. The circuit generates multiple 8-bit words with dynamic word-length control. The paper discusses the fabrication technology, the design of the word generator and its building blocks, and the performance of the complete chip.**

I. INTRODUCTION

FUTURE high-speed digital electronic systems, such as fiber-optic communication networks or radar signal processors, will require test instruments that generate, receive, and analyze data at rates greater than 1 Gbits/s. These needs can be met with GaAs monolithic-integrated circuits that operate at clock frequencies beyond the reach of present silicon IC's. The principal requirements for these GaAs circuits in test instrumentation are as follows:

1) short gate delays and fast rise and fall times (<100 ps) for full logic swings;

2) minimum switching time jitter (e.g., minimum phase noise in digital frequency dividers [1]);

3) compatibility with ECL families;

4) stable and reliable operation with adequate noise margins;

5) sufficient level of complexity to allow useful test circuits to be realized (100 to 1000 devices per chip);

6) reasonable power dissipation per chip (<2 W); and

7) high fabrication yield in order to be cost-effective.

Among the most useful circuits for test instrumentation having the above applications and requirements are pro-

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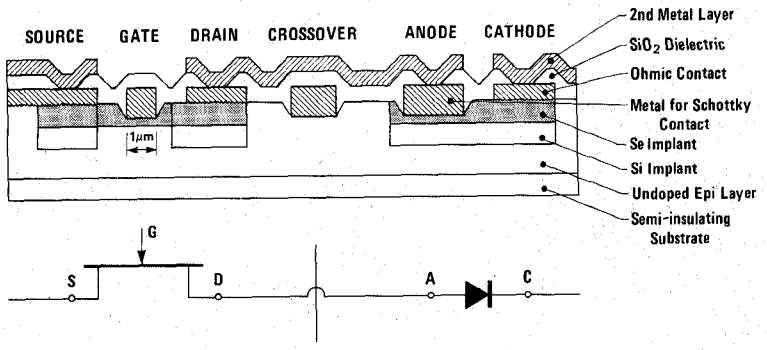

Fig. 1. Cross section of an integrated circuit section showing a transistor, a diode, and an interconnect line with crossover.

grammable word generators. Such circuits typically gather data, from a memory or a digital processor, and, by multiplexing techniques, generate high-speed serial bit streams. In general, it is desirable to form the data into words whose content, number, and overall duration can be dynamically controlled. A GaAs chip has been designed that meets these requirements. This circuit operates as an 8:1 multiplexer that generates multiple 8-bit words. The chip also incorporates timing and control logic that permit selective data blanking before and after words of 8-, 16-, 32-, 64-, or 128-bit length. In the word generator system application, a high-speed silicon IC provides the parallel input data. The GaAs multiplexer performs the critical parallel-to-serial data conversion, receives data at the maximum rate that the silicon circuit can deliver, and combines them on a single output channel. The GaAs IC is, therefore, the key component which extends the frequency capability of the entire system. It enables the equipment designer to achieve the highest possible data rate and a very "clean" waveform at the output.

Our GaAs IC development program started in 1973 with the demonstration of 80-ps propagation delay in GaAs logic gates [2] and continued with the design of monolithic 4-GHz (static) frequency dividers and of a counter/timer circuit with 150 devices [3]. This program has progressed to a successful evaluation of several MSI circuits that incorporate over 500 active devices and operate at multi-Gbits/s data rates. One of these circuits, the 5-Gbits/s word generator reported here, is four times faster than a recently reported GaAs multiplexer [4] and approximately twice as fast as the highest-speed silicon SSI counterpart [5]. In contrast to other GaAs IC development efforts [4], [6]–[9], no attempt was made to reduce power dissipation per gate to an LSI-compatible level. In our approach, it was considered more important to utilize the available power budget per chip (2 W) and design the logic gates for maximum speed [10]. Equally important are large noise margins which guarantee high functional yield (low cost) and reliable operation over a wide range of operating conditions.

In the following sections of this paper we outline the technology that was used (Section II), discuss the design of elementary building blocks (Section III), describe the operation of the word generator (Section IV), and report the measured chip performance (Section V).

II. Fabrication Technology

Fig. 1 shows cross sections of a transistor, a diode, and interconnections as implemented with this integrated circuit technology. The wafer is an undoped, high-purity semi-insulating substrate pulled in a B_2O_3-encapsulated Czochralski reactor under two atmospheres of N_2. The substrate's (100) surface is covered with a 3-μm-thick, undoped liquid-phase epitaxial layer grown in a horizontal slider reactor at 700°C. At 77 K, this high-purity buffer layer exhibits a Hall mobility greater than 120 000 $cm^2/V \cdot s$. The MESFET channel is formed by localized implantation of 500-keV Se ions into the buffer layer, at 350°C, to a dose of 6×10^{12} cm^{-2}. A 0.8-μm-thick Al mask is used to define the implanted regions. The resulting channel layer is 0.25 μm deep with a peak concentration of 2.5×10^{17} cm^{-3}. The associated sheet resistance of this region, 320 $\Omega/\square$, is very uniform with a 2 percent standard deviation over a 1×1 in wafer area. A second localized implantation is performed in order to lower the sheet resistance in the active area of diodes and under ohmic contacts. For this purpose, Si is implanted at 500-keV energy to a 1×10^{13} cm^{-2} dose. Both implants are simultaneously annealed under a Si_3N_4 protective cap at 850°C for 15 min. The ohmic contacts are processed in a conventional way by multilayer evaporation of NiCr, Ge and Au, lifting, surface capping with SiO_2, and alloying at 460°C. The specific contact resistance is 2×10^{-6} Ω cm^2. The gate is a 1.0 μ-thick Cr–Pt–Au metal stripe, recessed by 0.12 μm below the surface, and lifted with a combination of two positive resist layers (PMMA and Kodak 809). This processing step determines to a large extent the fabrication yield for the completed IC. On a typical wafer, one out of 3000 lifted gates (average gate width: 30 μm) is defective. The gate is recessed to reduce modulation of the drain current due to changing depletion layer widths under the "unpassivated" GaAs surface during switching transients. The gate metal is also used for first-level interconnections. Next, a dense SiO_2 layer is magnetron-sputtered onto the wafer resulting in a film with 1-μm thickness, 3.8 relative dielectric constant, less than 1 pinhole per cm^2, and with excellent coverage of vertical metal steps. Via holes of $2\ \mu m\times3\mu m$ area are etched into the SiO_2 with 45° tapered slopes. Finally, a Ti–Pt–Au second metallization layer is deposited, 1 μm thick, and patterned by Ar ion-beam milling.

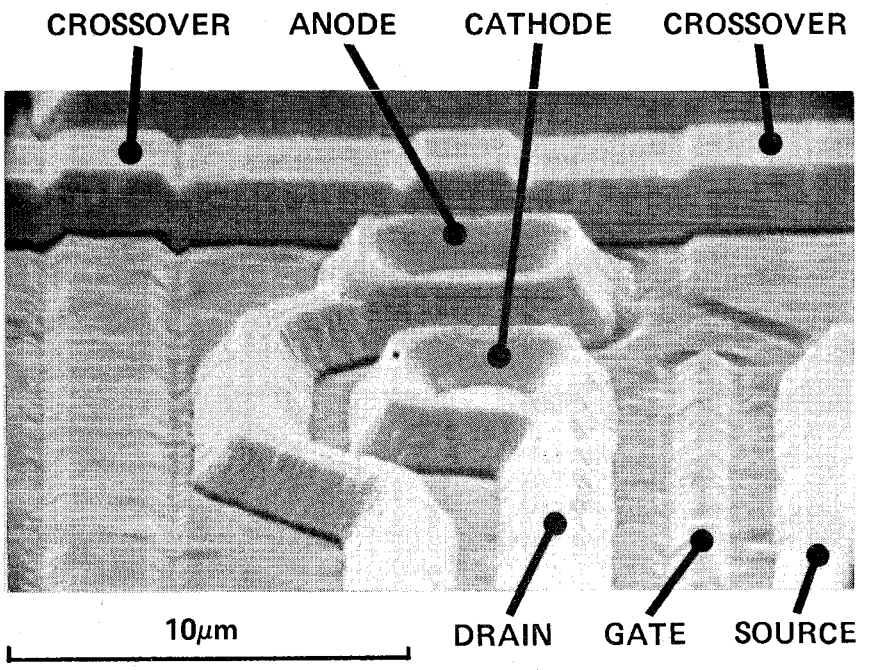

Fig. 2. Scanning-electron micrograph of an IC section showing a transistor, a diode, and various interconnect lines.

A scanning electron micrograph of a completed circuit is illustrated in Fig. 2. This figure shows all the essential circuit elements: a transistor, a diode, and various interconnect lines in first and second metal layers. Noteworthy features are: 1) the high packing density of components; 2) the tapered edges of the via openings; 3) the slanted SiO_2 surfaces covering vertical gate and ohmic metal edges; and 4) the step coverage of the second metal at crossover points. These MSI circuits with 500 active components have been fabricated with a functional yield of 30 percent.

III. Logic Gates and Flip Flops

The basic NAND/NOR logic gate uses parallel-connected single-gate or dual-gate drivers, an active pull-up load, three level-shift diodes, and a pull-down current source. A 1-mm-wide single-gate driver has the following characteristics at zero gate voltage ($V_{GS}=0$): 200-mA saturated drain current, 130-mmho transconductance, 1.8-V gate-cutoff voltage, 1.4-pF gate-to-channel capacitance ($V_{DS}=0$), 0.2-pF drain-to-source capacitance ($V_{DS}=2$ V), 4-Ω drain-to-source resistance at zero drain voltage ($V_{DS}=0$), and 90-Ω resistance in the saturated current region ($V_{DS}=2$ V). Based on these MESFET characteristics, the transistor gate widths of the basic logic gate have been computer-optimized to achieve the fastest, yet equal, rise and fall times at the output. The measured data of the resulting (standard) logic gate with 16-μm driver transistors and +4.5 V/−3.5 V dc supply voltages are: 2.5-V logic swing, 0.9-V noise margins, 10-dB voltage gain in the transition region, 10-mW power dissipation, and 60-ps propagation delay for unity fan-in and fan-out.

Another basic building block is the *D*-type flip-flop shown in Fig. 3. A complementary-clock circuit has been chosen because of its high-speed capability [3]. During the course of this work, several complementary-clock circuit versions have been computer-optimized and experimentally tested. The version in Fig. 3 allowed the fastest clocking rate.[1] The maximum clocking rate is high in this circuit because the signal from the data amplifier's input to the latch input (D to $\overline{M}$, in Fig. 3) traverses only a single gate's delay path. The latch, which shares common output nodes with the data amplifier, is disabled by the complementary clock ($\overline{CK}$: low) during data entry. An identical configuration in the slave also insures settling within one gate delay, τ_p. The maximum toggle rate is, therefore, $f_c=1/(2\tau_p)$. It should be noted that only single-gate transistors, operating in a differential mode, are utilized.[2]

The performance of the *D* flip-flop, as well as all other subcircuits in the word generator, were extensively simulated on SPICE [11], using the model developed by Van Tuyl [12]. MESFET gate widths and diode parameters were carefully chosen to insure stable operation of the flip-flop for a given range of bias voltages and phase differences between the complementary clocks. In the computer-aided design, special attention was given to the generation of "clean" waveforms with fast transition times over a wide range of clock rates. Fig. 4 shows the computed and measured output waveforms for the flop-flop when operated as a 2:1 frequency divider with a 3.3-GHz sinusoidal clock. The output waveforms are nearly identical; they show 80-ps rise and fall times, the same ripple characteristics in the low and high states, and a slightly longer duty cycle in the high state. Clean and stable waveforms have

[1]This circuit is similar in topology to a well-known ECL flip-flop. R. Van Tuyl is credited for implementing this circuit for the first time in GaAs in 1975.

[2]The dual-gate FET can be analyzed as two single-gate transistors in series. The transconductance of the upper FET is degraded by the negative feedback of the lower FET's ON-resistance.

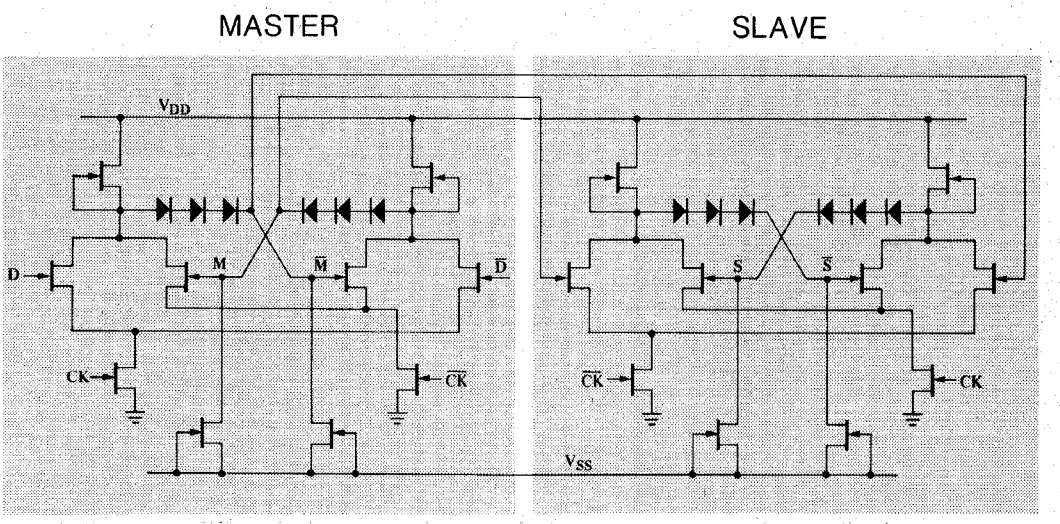

Fig. 3. D-type master–slave flip-flop used in the timing circuit of the word generator.

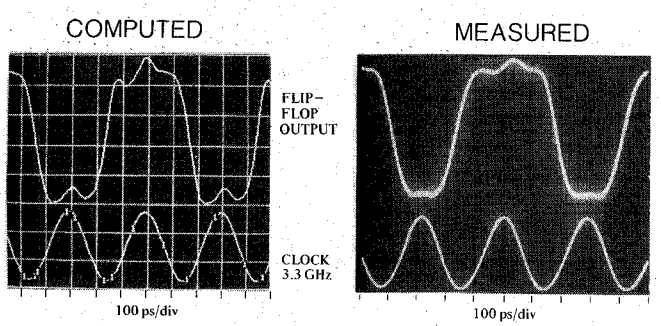

Fig. 4. Computed and measured output waveforms of a 2:1 flip-flop frequency divider for a 3.3-GHz sinusoidal clock.

been obtained for clock frequencies from a few Hertz up to 5 GHz. Measurements on selected wafers have demonstrated toggling rates up to 6.5 GHz.

IV. Logic Design of the Word Generator

In the system application, the GaAs IC operates as the highest speed component in a hybrid circuit that consists of a GaAs chip and a silicon emitter-coupled logic (ECL) chip. The silicon IC is a data generator that produces independently-selectable words in eight parallel output channels. These words are fed to the data inputs of the GaAs chip which operates as an 8:1 parallel-to-serial data converter.

The logic block diagram of the GaAs IC is shown in Fig. 5. The data in the eight input channels are first amplified in the interface circuits, labeled *I*. A tree of 2:1 multiplexers (MUX) connects the eight inputs to the single output in a time-multiplexed sequence. The last block in the data path is an output buffer amplifier with 50-Ω output impedance that feeds pulses of 0.7-V amplitude into a 50-Ω transmission line. The switching of the individual multiplexers is controlled by a timing generator that receives its input from an external clock. The timing generator produces four-phase timing signals for the multiplexers in the first row, two-phase signals for the second row, and a delayed clock signal for the third row. In many applications, single words of variable length must be generated

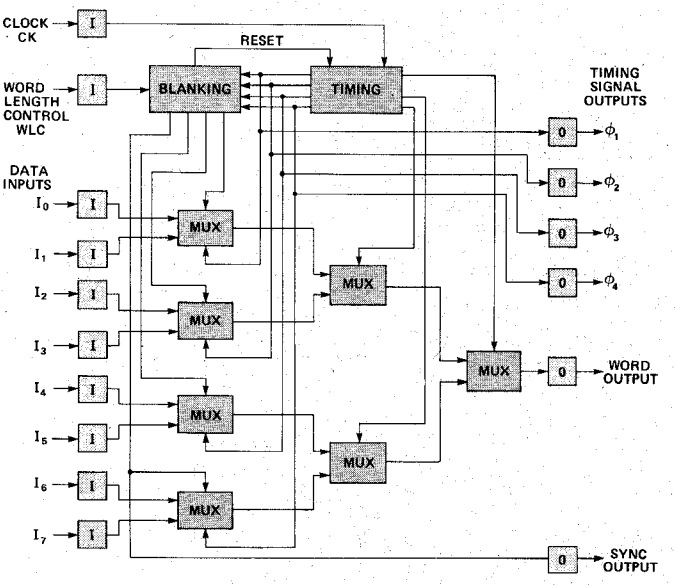

Fig. 5. Block diagram of the word generator showing input amplifiers (I), 2:1 multiplexers (MUX), output amplifiers (O), blanking and timing circuits.

and the output must be clamped to the zero level before and after the word appears. In this circuit, an input pulse defining the word length is fed to a control circuit that generates blanking signals for the four input multiplexers.

Fig. 6 shows the logic circuits for the 8:1 multiplexer. The input data are amplified in three inverter stages that convert the ECL inputs to the 2.5-V logic swing used within the GaAs IC. The multiplexers in the first row are 5-input AND/OR/INVERT gates with amplified input data, timing signals, and blanking signal as inputs. The multiplexer in the third row, labeled *XO*, must operate at the highest speed. It critically influences timing accuracy, pulse symmetry, and transition times of the output data. Therefore, a special design, shown in Fig. 7, has been adopted. This stage incorporates the data selection function into a pair of high-speed differential amplifiers. The differential amplifiers exhibit a higher speed during clock transitions than that available from the AND/OR/INVERT gates used

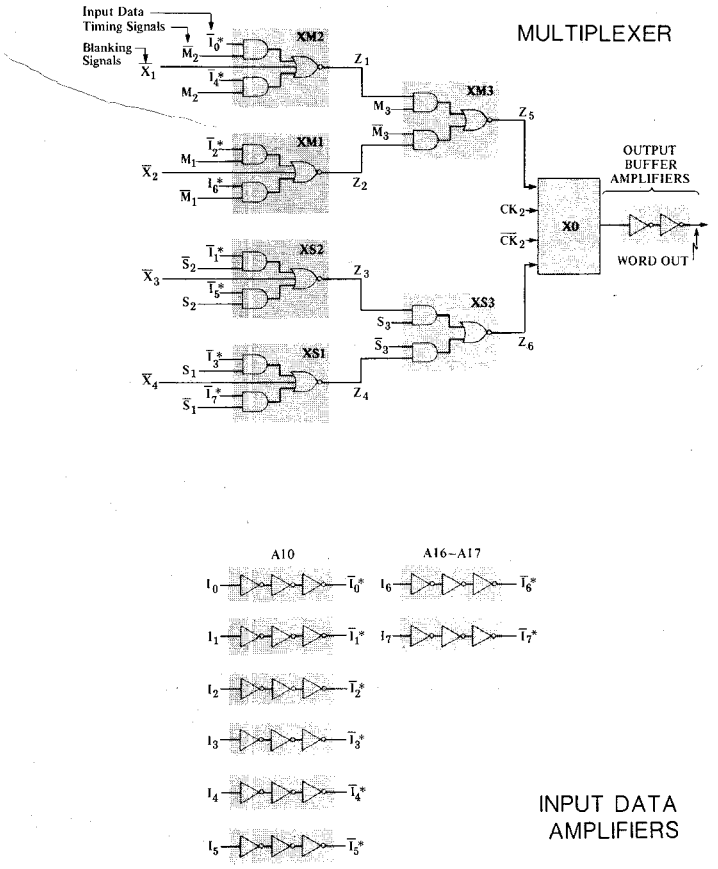

Fig. 6. 8:1 multiplexer and input amplifiers of the word generator.

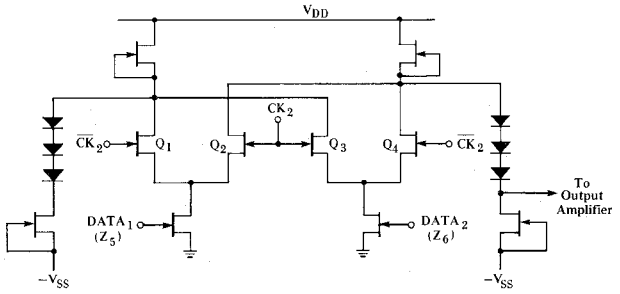

Fig. 7. Final multiplexer stage XO.

throughout the other two levels of multiplexing. Complementary clocks $CK_2, \overline{CK_2}$ used at the input to XO are delayed versions of $CK_1, \overline{CK_1}$, and are applied from separate inputs to the chip. This provision allows one to compensate for the delays through gates $XM3$, $XS3$, and thereby optimize the data selection in XO.

Fig. 8 illustrates the circuit realization for the timing generator and blanking control. The timing generator consists of a synchronous divide-by-four counter (flip-flops $F1$ and $F2$) and a divide-by-two counter (flip-flop $F3$). The outputs from flip-flops $F1$ through $F4$, M_i and S_i ($i = 1 \cdots 4$), are from the master and slave, respectively. These outputs, shown in the timing diagram of Fig. 9, are applied to the multiplexers ($XM1$, $XM2$, $XM3$ and $XS1$, $XS2$, $XS3$)

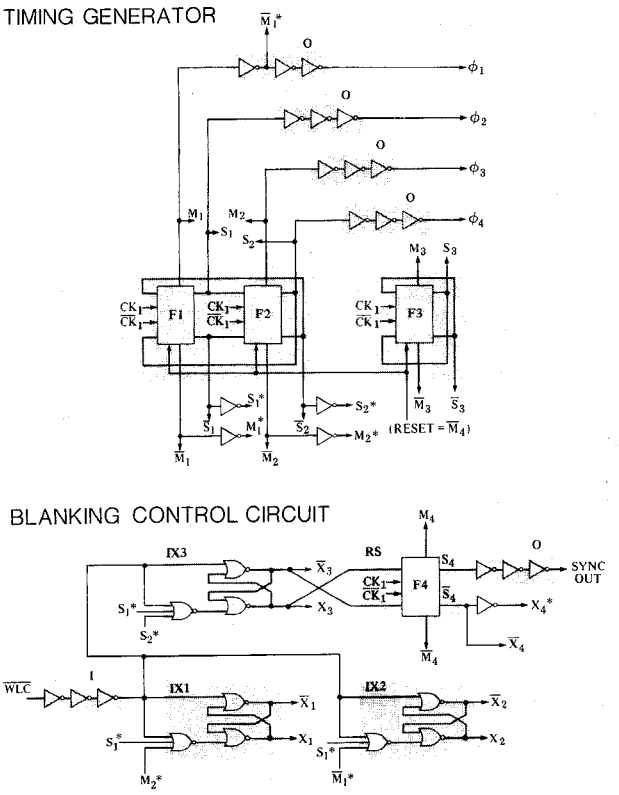

Fig. 8. Timing and control circuits of the word generator.

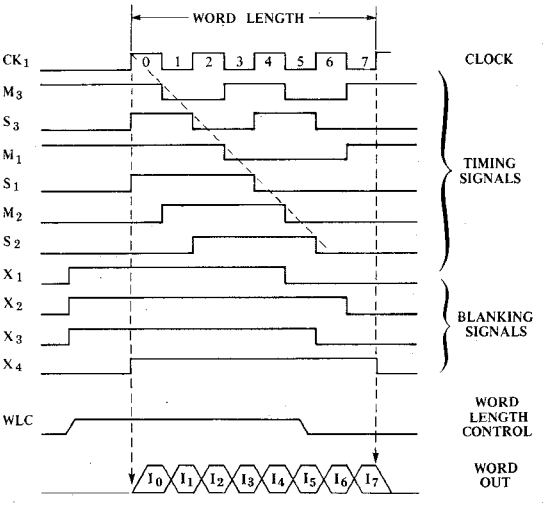

Fig. 9. Timing diagram for the word generator.

in a specific sequence that eliminates glitches in the output data, due to skew in gate propagation delays. The four-phase timing signals $\phi_1 \cdots \phi_4$ are amplified and are available with 0.7-V amplitude (into 50 Ω) for synchronous clocking of the preceding silicon IC.

The blanking control circuit consists of flip-flop $F4$ and latches $IX1$, $IX2$, and $IX3$, shown at the bottom of Fig. 8. Before the application of the word length control (WLC) pulse the multiplexers' outputs are locked to the logic zero level independent of the input data. When WLC makes a transition from low to high, the blanking signals X_1, X_2,

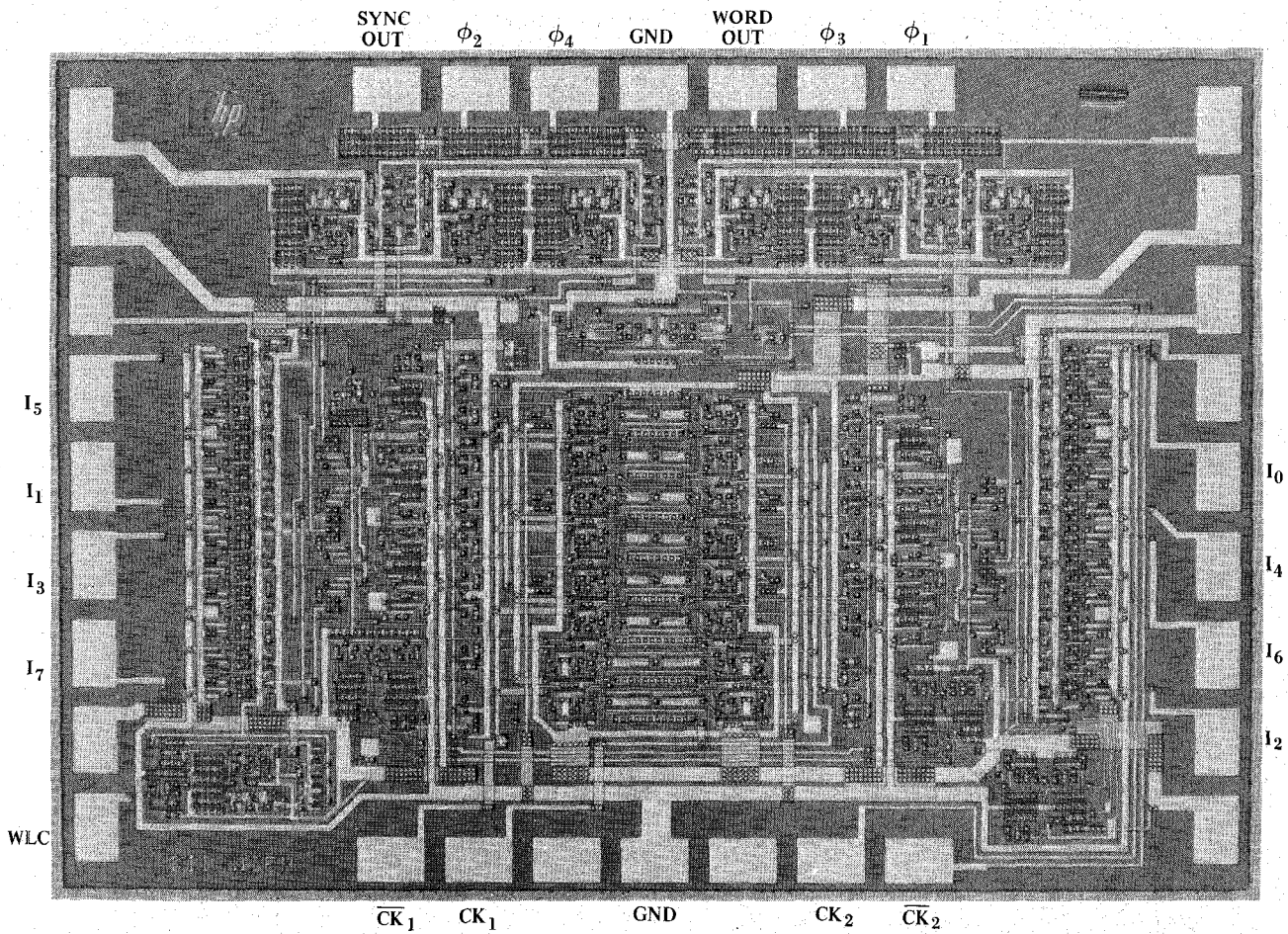

Fig. 10. Photomicrograph of the 1.1-mm×1.6-mm word generator chip. Timing generator occupies the center of the chip, input amplifiers and multiplexer tree border on each side, output amplifiers are at the top.

and X_3 begin to enable the multiplexers as shown in the timing diagram of Fig. 9. The edge of the word length control pulse defines the start of the word on the next rising clock edge. The eight input channels are then alternately connected to the output. The word-length control pulse does not have to pinpoint the end of the word accurately; it only has to switch during the last sequence of 4 bits. The blanking control logic defines the end of the word in a way that words are always composed of multiples of 8 bits.

The circuit chip, shown in the photomicrograph of Fig. 10, measures 1.1 mm×1.6 mm in size, carries 32 contact pads, and incorporates 400 transistors (MESFET's) and 230 Schottky diodes. The input amplifiers are next to the pads on the left and right side, and the output amplifiers are at the top of the chip. The timing generator is in the center, surrounded on three sides by the 2 : 1 multiplexers.

V. Performance of Word Generator

For measurements, the chip is mounted in a microwave package as illustrated in Fig. 11. The chip, which dissipates 1.9 W, is soldered onto a heat sink. The two ground pads are connected directly to the RF-grounded heat sink. The remaining 30 contact pads are thermo-compression bonded to 50-Ω microstrip lines, printed on 50-μm-thick Kapton (polyimide). This package introduces low insertion loss (<1.2 dB) and low capacitive coupling between adjacent lines (< −28 dB) up to 14 GHz. A more detailed description of the design and performance of this IC test package will be presented in a forthcoming publication [13].

An example for the generation of a 32-bit word at a low data rate (1 kbits/s) is shown in Fig. 12. The WLC is stepped from 0 to 1, and the first rising edge of the clock burst starts the word. Thereafter, the stationary input data (10100101) is repeated at the output four times in non-return-to-zero (NRZ) format. During the fourth sequence of 8-bits, the control pulse returns to the logic 0 level, identifying the last group of 8 bits. A 32-bit word, generated at a high data rate (2 Gbits/s), is demonstrated in Fig. 13. The upper trace identifies the WLC with its slow transitions (0.8 ns). The lower trace shows the resulting word in which the 10100011 sequence is repeated four times.

The key features of the GaAs IC multiplexer are its speed and its capability of generating clean waveforms with fast transition times. These characteristics are illustrated in Fig. 14, where the output-voltage waveform is

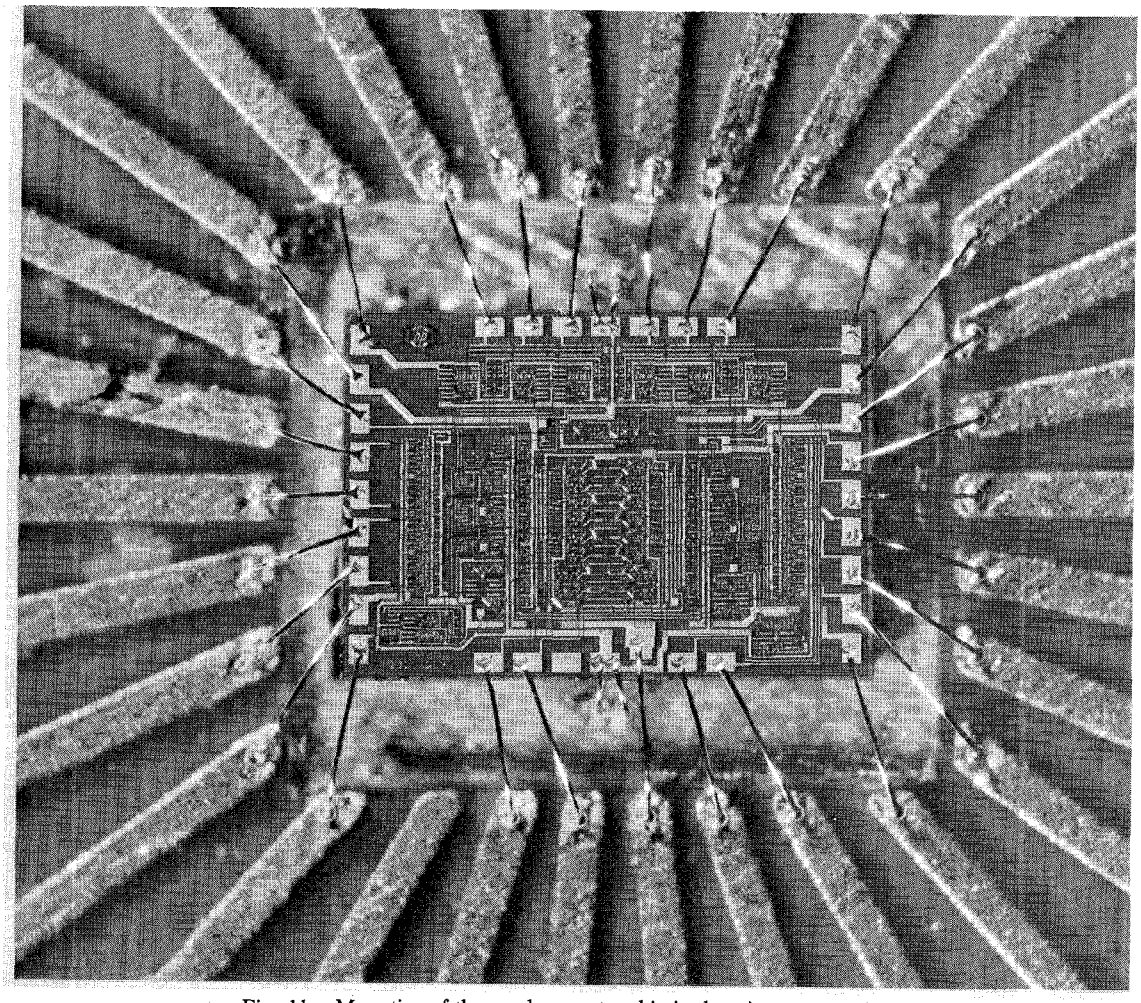

Fig. 11. Mounting of the word generator chip in the microwave package.

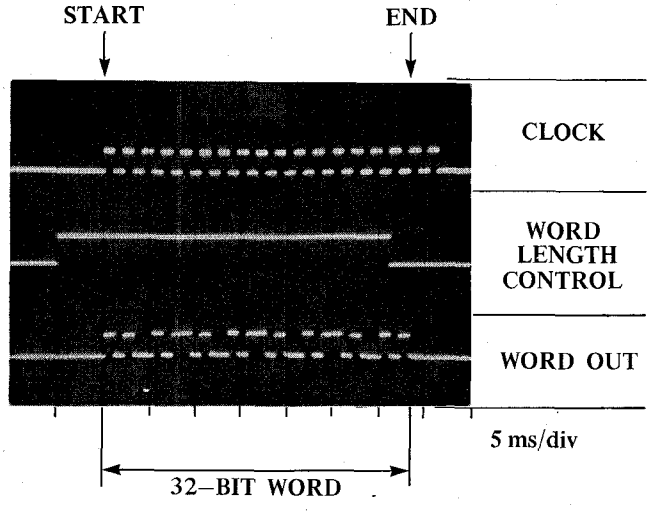

Fig. 12. Generation of a 32-bit word at 1 kbits/s.

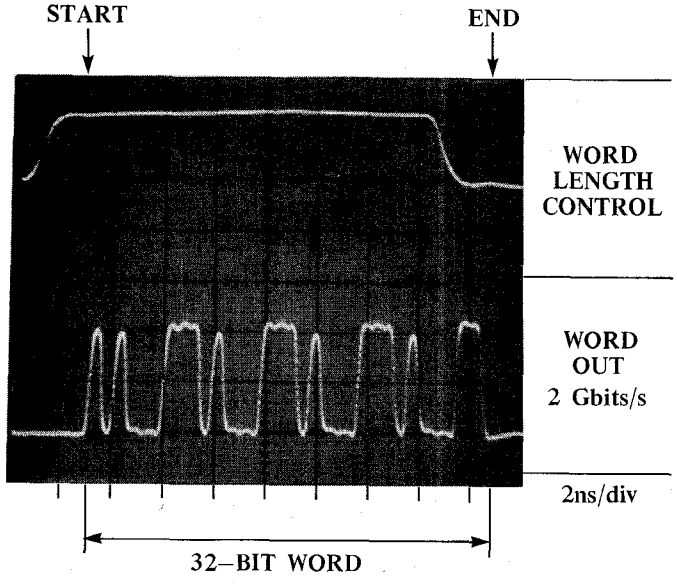

Fig. 13. Generation of a 32-bit word at 2 Gbits/s.

shown at a date rate of 5 Gbits/s. Even at this extremely high data rate, the circuit is perfectly stable; the waveforms are very clean with no "glitches", and with negligible overshoot, "ringing", and time jitter. The voltage rises and falls with 100-ps transition time. The maximum speed performance, shown in Fig. 14, is obtained for a data sequence of infinite length. By changing the clock

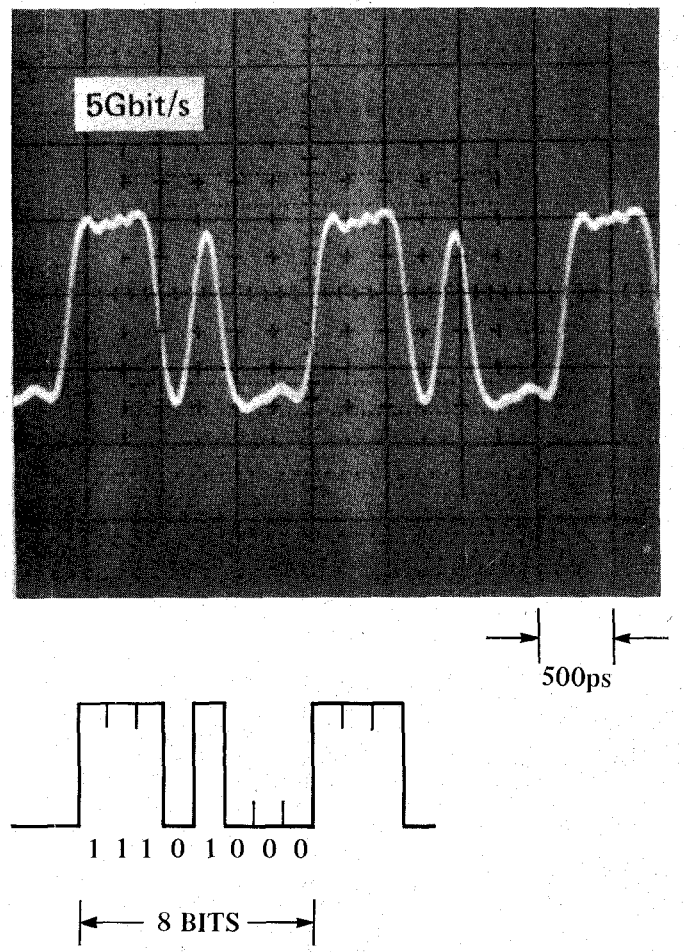

Fig. 14. Output waveform at 5-Gbits/s data rate.

frequency, the output data can be varied from a few bits/s up to 5 Gbits/s while maintaining perfect stability at all frequencies.[3]

VI. Conclusions

A practical technology base has been established for GaAs IC design and fabrication. Several MSI circuits with over 500 active components have been built and successfully tested [13], [14]; one of these circuits, a 5-Gbits/s word generator, is described in this paper. This IC demonstrates the capabilities and potential of this technology with depletion-mode transistor logic. The outstanding merit is the high-speed performance that is clearly beyond the reach of present silicon-based IC's.

Chips have been evaluated from 30 wafers. The results show that a) 30-percent functional yield can be obtained for these MSI circuits, and b) gigabit per second performance with stable and reliable operation is repeatable. The reported data are not based on characteristics of a unique wafer or unusual chip. The stable and reproducible circuit performance is largely due to the fact that a conservative approach for design, layout, and processing was adopted. The confidence in this approach was established from prior evaluation of test patterns and circuit building blocks. Furthermore, these IC's are easy to interface with existing ECL families.

It is anticipated that the GaAs IC technology will offer a cost-effective approach for medium-scale-integrated circuits in new high-speed systems. Results reported in this paper establish a starting point. Further advances in lithography (direct *E*-beam writing), surface passivation, channel-to-substrate interface stabilization (backgating, carrier trapping, space-charge-limited current flow), and in-device parameter control will lead to significantly higher speed, lower power consumption, and larger circuit complexity in the near future.

[3]Operation down to very low frequencies is possible as long as the edges of the input clock are sufficiently fast (< 2 ns).

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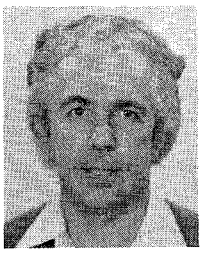
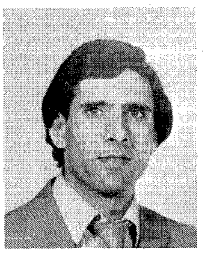
Mr. Gowen has been affiliated with the Hewlett–Packard Company, Palo Alto, CA since 1960. He is responsible for the chemical processing of a wide variety of semiconductor devices.



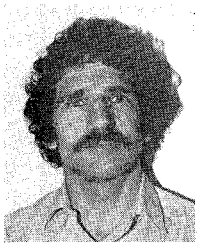
Robert Joly received degrees in mechanical engineering and electrical engineering in France in 1957 and 1959, respectively, and the Ph.D. degree in electrical engineering from Stanford University, Stanford, CA, in 1970.

He performed research and development on radar at Thomson C.S.F. before joining the Microwave Division, Hewlett–Packard Company, Palo Alto, CA. In 1978 he transferred to Hewlett–Packard Laboratories where he was involved in the development of cryogenic devices and in high-speed gallium arsenide integrated circuits.



Masood Namjoo was born in 1953 in Iran. He received the B.S. degree in 1977 from Tehran Institute of Technology, Iran, and the M.S. degree in 1979 from Stanford University, CA, both in electrical engineering. He joined Hewlett–Packard Solid-State Laboratory in 1979 where he was mainly concerned with the computer design and evaluation of medium-scale GaAs digital IC's.

Presently, he is consulting for the Hewlett–Packard Company and is also a Ph.D. student at Stanford University. His area of research at Stanford is digital systems reliability. He expects to receive his Ph.D. degree in 1982.



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Mr. Podell holds twenty patents in diverse areas and has published or presented a number of technical papers.